A Survey of the Implementation of Linear Model Predictive Control on FPGAs

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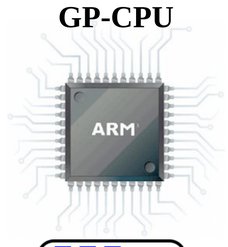
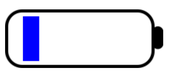
Optimal Control Problem

- Constrained Linear Quadratic Regulator

$$\begin{aligned} \underset{u,x}{\text{minimize}}\ & \|x_N\|_P^2 + \sum_{k=0}^{N-1}\left(\|x_k\|_Q^2 + \|u_k\|_R^2\right) && \}\text{Quadratic cost function} \\ \text{subject to}\ & x_{k+1} = Ax_k + Bu_k,\ k = 0,\dots N-1 && \}\text{Linear prediction model} \\ & Fu_k \leq c_u,\ k = 0,\dots N-1 && \}\text{Input constraints} \\ & Dx_k \leq c_x,\ k = 1,\dots N && \}\text{State constraints} \end{aligned}$$

- Solution found by solving a convex quadratic program

Computing Devices

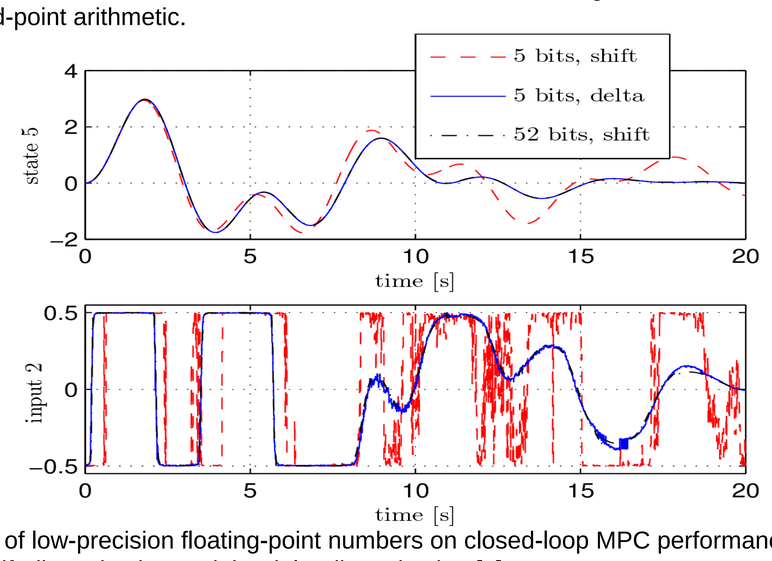
	GP-CPU	GPU	FPGA
			
Power Requirements			
Architecture	Sequential	Parallel	Customizable
Peak FLOPS	100M-100G	100G-3T	10T
MPC Research	Popular	Limited	Popular

Number Representation

- The closed-loop performance of MPC may degrade in reduced-precision
- Algorithms must be stable under reduced-precision
- Prefer algorithms with bounds on variable values to reduce likelihood of overflow in fixed-point arithmetic

	Fast Gradient Method	Alternating Direction Method of Multipliers	Dual Gradient Projection	Proximal Newton Method
Stable Under Roundoff Errors	✓	✓	✓	✓
Data-Type Size Rules	✓	✓	✓	✓
Upper Iteration Bound	✓	✗	✓	✓

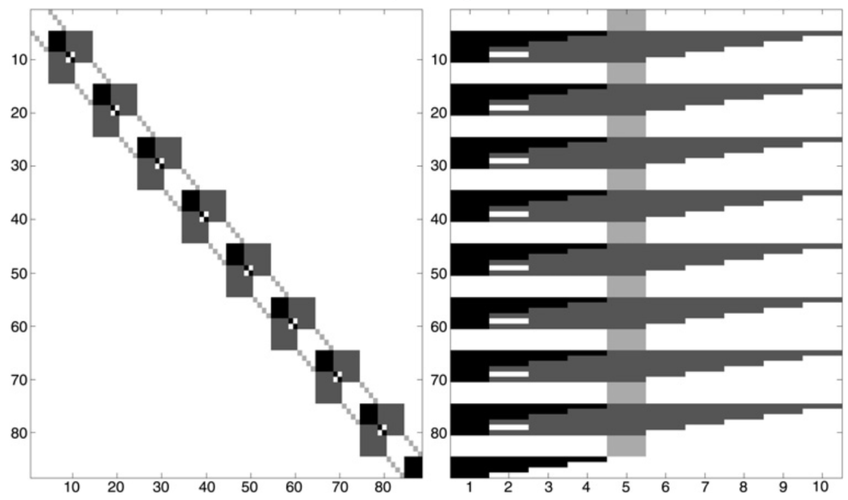
The existence of theoretical results for various first-order algorithms when used in fixed-point arithmetic.



Effect of low-precision floating-point numbers on closed-loop MPC performance using the shift discretization and the delta discretization [1]

Memory Architectures

- Exploit structure to reduce memory usage and improve scalability



Sparse KKT matrix (left) and a possible storage pattern (right) that only stores the non-zero diagonals [3]

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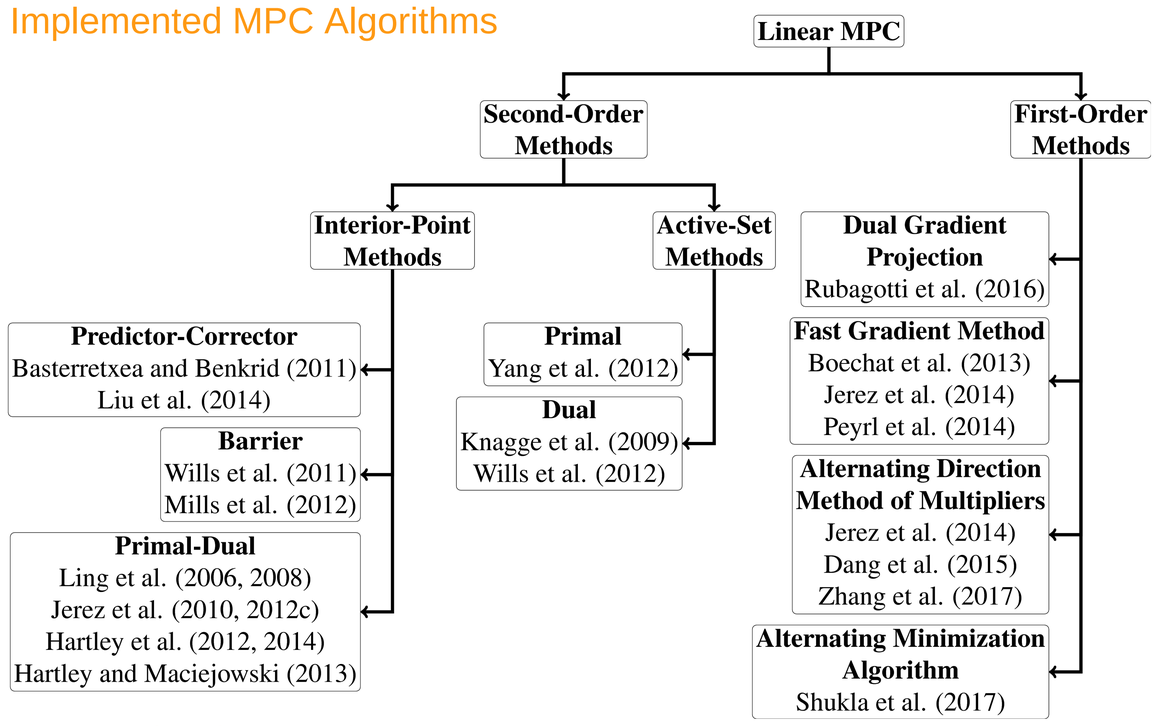
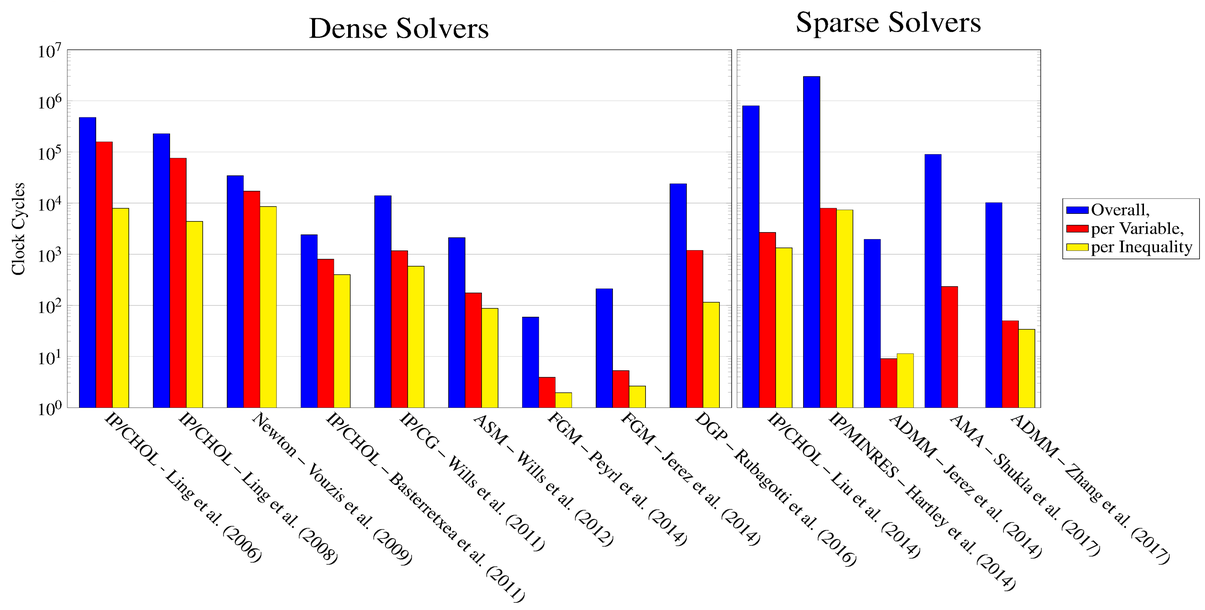
Implemented MPC Algorithms

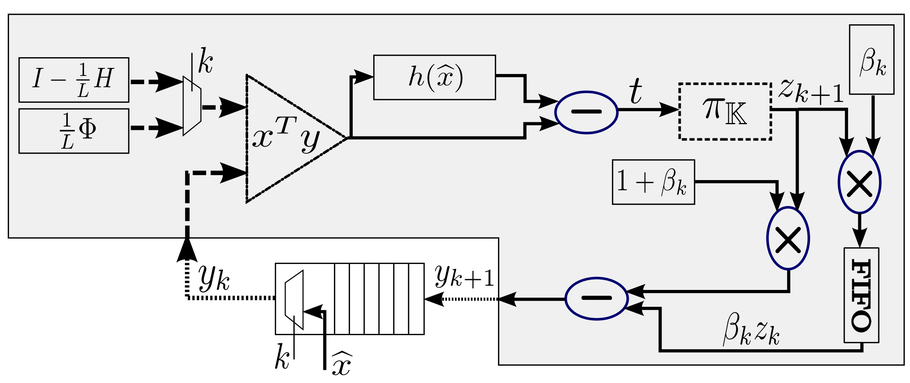


Reported Solver Performance



Computational Units

- Low-level linear algebra easily parallelized for both first-order and second-order methods
- Algorithm-level parallelizations implemented primarily for first-order methods



Computational unit for a single variable in a Fast Gradient Method Implementation [2]. Multiple units can be used to process multiple variables in parallel.

Future Research Directions

- User-friendly code-generation utilities for FPGAs
- Using High-Level Synthesis tools for implementations
- Hardware-software co-design optimization
- Heterogeneous processor systems & computational resource allocation

Open questions for nonlinear MPC on FPGAs

- What algorithmic parallelizations can be exploited?
- How does reduced-precision affect nonlinear discretization schemes?
- How can mesh-refinement be efficiently handled on embedded systems?
- How can nonlinear functions be implemented efficiently?
- How should the matrices be structured in memory to improve performance and scalability?

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